IN THE SPECIFICATION

Please amend the specification as follows.

In the "Brief Description of the Drawings" section, please amend the fourth paragraph starting at page 2, line 25 as follows:

Fig. 3 illustrates an exemplary decimate-by-four polyhase filter structure; and

In the "Detailed Description" section, please amend the fourth paragraph starting at page 3, line 13 as follows:

The input data enters the delay line on the left side of Fig. ~~2~~ 3. On each clock cycle all the data shifts over one delay to the right and the new input enters on the left, the data are shown as s0-s7 in Fig. 2 ("s" is an abbreviation for sample). The content of each delay element is multiplied by an associated fixed coefficient, labeled c0-c7 in Fig. 2 ("c" is an abbreviation for coefficient). All the multiplier outputs are summed to form the filtered result.

Please amend the Abstract as follows.

Parallel adaptive filters and filtering methods that enable processing of an input signal in a circuit that has an clock speed many times slower than the input rate of the input signal that is processed. ~~The present invention extends the use of a~~ A polyphase decimator structure ~~to~~ processes a data stream requiring a low pass filtered bandlimited (low-rate) output that is used for high-rate output structures. The filters and methods break an input data stream into parallel paths that efficiently produce a bandlimited (decimated, low-rate) filtered output. Each of the parallel paths is processed at a decimated rate to provide a filtered output signals corresponding to a filtered version of the input signal.